REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-44 are pending in the application. Claims 1-44 have been rejected.

CLAIM REJECTIONS

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1,12,23,24,26,27,34,35,37 and 38 under 35 U.S.C. § 102(b), as allegedly being anticipated by Sauer et al. (U.S. #5,973,311). Applicant respectfully traverses the Examiner's rejection in view of the remarks that follow.

Applicant asserts that The Examiner's "broad definition" of a Direct Injection unit cell in the Office Action is incorrect. While, as the Examiner indicates that the present specification does not provide a definition of Direct Injection circuits (also termed in the industry as "di", "DI', "di readout circuit", "DI readout circuit", "Active Pixel Sensor (APS) cell di readout circuit", or "Active Pixel Sensor (APS) cell DI readout circuit", Applicant asserts that there was no need to provide such a definition since the definition of the term "Direct Injection" is a well known industry standard. Applicant would like to draw the Examiner's Attention to a review of circuit designs in the imager industry. The citation is from pages 23.19 and 23.21 of chapter 23 entitled "Infrared Detector Arrays" from of the "Handbook of Optics", Volume I, (Second Edition) Edited by Michel Bass (McGraw –Hill

Inc, 1995). A copy of pages 23.19 and 23.21 is attached herewith. In this review the Authors distinguish between different detector interface designs.

Circuit 9 (a) of Fig. 9 is a Direct Detector Integration (DDI) circuit (which is also known in the art as Source Follower per Detector (SFD) configuration) to which resembles the design used by Sauer et al. In this type of circuit as well as in the circuits disclosed by Sauer et al. (Differential Pair Source Follower configuration), the photodetector current develops a voltage which modulates the gate of an MOS type transistor (the readout circuit's input). The readout circuit's output signal is a modulated voltage developed over the CMOS transistor's source node. The reference node of this circuit is the CMOS transistor's drain node, which is appropriately biased around the circuit's quiescent point and which does not vary with the photo-detected signal. The developed output voltage follows the input gate's voltage. **The term "Direct Detector Integration" indicates that the photo-detected charge gets integrated directly on the photodetector - prior to being output on the source node.** This circuit belongs to the so called "Common Drain" amplifiers class. The examiner Attention is also directed to Kenneth R. Laker, Willy M.C. Sansen: "Design of Analog Integrated Circuits and Systems", pp. 292-299, McGraw-Hill, 1994, a copy of which is also attached herewith, which discusses the Source Follower circuit. From the simplified circuit's model Figure 4-19 (of Laker and Sansen) one can easily deduce that the Source Follower is an ideal voltage buffer, as it transforms a high internal impedance voltage signal into almost identical in magnitude output signal with low internal impedance. This facilitates the almost lossless transfer of the photo-detector developed directly integrated signal to the sensor's output. The Sauer et al. circuit as well attempts to take further the concept of the DDI circuit of Fig. 9(a) (of Handbook of Optics), by replacing the single Source Follower with a differential pair circuit, which sums up two output voltage sources on the joint source node. However, since the output impedance of each of the output signals is similar, the circuit averages the two output voltage signals while the noise goes up (it is the square root of the sum of squares of each noise voltage source) in the Sauer Circuits, or a voltage signal is presented to the MUX input (in Fig. 9(a)), **there is no charge summation or direct charge transfer whatsoever on the column line.** In short, rather than improving the Signal to Noise ratio, the Sauer et al circuit causes the deterioration of the SNR, thus defeating its original purpose (and is therefore useless).

In contrast to the above, (and not to be mixed with the term "Direct Detector Integration or DDI), the circuit of Fig. 9(b) (of the Handbook of Optics reference) as well as in the unit cell circuit of the present invention is a Direct Injection (DI) circuit. The photosensor's developed current signal is input (injected) directly into the MOS transistor's source node. The output signal which is a current almost identical to the input current, is developed on the CMOS transistor's drain node. This drain current creates charge integrated on the column line capacitor (and is NOT integrated on the photodetector's capacitor as in the DDI) also defined as the integration capacitor ($C_{storage}$ of Fig. 9(b), or CI_1, CI_2 etc. of the present invention). As may be observed from 9(b) the MOS transistor's gate is biased to a quiescent point voltage (the transistor's gate is connected to a fixed voltage V_{BIAS}), and does not develop a signal on the gate (which is done in the SFD/DDI circuit). The CMOS transistor in this cell is configured in a "Common Gate" configuration (the Examiner is further referred to Kenneth R. Laker, Willy M.C. Sansen: "Design of Analog Integrated Circuits and Systems", pp. 308-314, McGraw-Hill, 1994, which discusses the Common Gate or the interchangeably-used term MOST Cascade circuit. Figure 4-19 of this reference demonstrates that the Common Gate amplifier circuit emulates an ideal Current (and NOT voltage) Buffer. This circuit injects the photodetector's current into a low source input impedance and regenerates high output impedance current, which is almost the same as the photodetector's current signal. Due to this DI configuration the charge generated by the photosensor directly flows to and accumulates within the integration capacitor ($C_{storage}$ of Fig. 9(b), or CI_1, CI_2 etc. of the present invention), from which it may be transferred to the column capacitor by suitable switching of the readout transistors TR1, TR2 etc. The term "Direct Injection" or "DI" indicates that the photodetector's current (and also charge) is directly injected to the amplifier's input.

Applicant therefore asserts that the Examiner has mistakenly interchanged the term "DDI – Direct Detector Integration" (which is used by Sauer et al.) with the term "DI – Direct Injection (used in the circuits of the present invention) which terms are not interchangeable and are entirely different.

Applicant therefore asserts that the circuits disclosed by Sauer et al. are clearly of the DDI or SFD type as defined in the Handbook of Optics citation above and are not Direct Injection (DI) Circuits."

In view of the above remarks, Applicant asserts that Sauer et al. do not teach nor even fairly suggest "plurality of direct injection unit cells" recited in independent claims 1, 12, 23 and 34. Applicant respectfully assert that Sauer et al. does not teach nor does it even fairly suggest the direct injection unit cells or pixels as recited in claims 1, 12, 23 and 34. Moreover, Applicant respectfully requests the Examiner to point out where exactly in Sauer et al. specification and drawings does Sauer et al. disclose or teach a direct injection unit cell or pixel.

In view of the above remarks, Applicant respectfully asserts that independent claims 1 12, 23, and 34 are allowable over Sauer et al. Claims 24, 26, 27 depend from, directly or indirectly, claim 34 and therefore include all the limitations of this claim and are also allowable. Claims 35, 37 and 38 depend from, directly or indirectly, claim 34 and therefore include all the limitations of this claim and are also allowable.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. § 102(b) to independent claims 1 and to independent 23 and to claims 24, 26, 27, dependent thereon.

Similarly, for the same reasons indicated hereinabove, Sauer et al. cannot anticipate claims 12 and 34. Applicant respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. § 102(b) to independent claim 12 and to independent 34 and to claims 35, 37 and 38 dependent thereon.

Applicants respectfully request reconsideration and withdrawal of the rejections of claims 1, 12, 23, 24, 26, 27, 34, 35, 37 and 38.

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 2,4,5,13,15 and 16 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Kokie et al. (US #4,212,034)

Applicants respectfully traverse the rejection of claims 2,4,5,13,15 and 16 as being unpatentable over Sauer et al. in view of Kokie et al. (US #4,212,034) because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention. The combination of Sauer et.al. and Kokie et al., does not teach or even fairly suggest all the limitations of independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 2,4,5 and 13,15,16 depending, respectively, thereon. Sauer et al. has been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit does not teach "plurality of direct injection unit cells" as recited in independent claims 1 12, 23, and 34, the man skilled in the art would not have been motivated to combine Kokie et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Kokie et al with the source follower circuits of Sauer et al. which teaches away from charge summing (by using voltage averaging and not charge summing). Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 3 and 14 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Pain et al. (US #8,801,258).

Applicants respectfully traverse the rejection of claims 3 and 14 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Pain et al. (US #8,801,258), because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there

would have been motivation to combine them to form the claimed invention. The combination of Sauer et.al., Kokie et al., and Pain et al. does not teach or even fairly suggest all the limitations of independent claim 1 or of claim 12, nor does it teach or suggest all the limitations of dependent claims 3 and 14 depending, respectively, thereon. Sauer et al. and Kokie et al. have been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit does not teach nor even fairly suggests the "plurality of direct injection unit cells" as recited in independent claims 1 12, 23, and 34, the man skilled in the art would not have been motivated to combine Kokie et al. and Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Kokie et al. and Pain et al. with the circuit of Sauer et al. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 6, 7, 17, 18 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al., Kokie et al., Pain et al., and further in view of Nishida et al.(US#4,996,600).

Applicants respectfully traverse the rejection of claims 6, 7, 17, 18 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al., Kokie et al., Pain et al. and further in view of Nishida et al. (US#4,996,600), because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., Kokie et al., Pain et al. and Nishida et al. does not teach or even fairly suggest all the limitations of independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 6,7 and 17,18 depending, respectively, thereon. Sauer et al., Kokie et al. and Pain et al. have been discussed above. That discussion is applicable here.

The combination of Sauer et.al., Kokie et al., and Pain et al. and Nishida et al. does not teach or even fairly suggest all the limitations of independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 3 and 14 depending, respectively, thereon. Sauer et.al., Kokie et al., and Pain et al. have been

discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit does not teach or even fairly suggests the "plurality of direct injection unit cells" as recited in amended independent claims 1 12, 23, and 34, the man skilled in the art would not have been motivated to combine Nishida et al, Kokie et al. and Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Nishida et al., Kokie et al. and Pain et al. with the circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 8-11, 19-22 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Nishida et al.(US#4,996,600).

Applicants respectfully traverse the rejection of claims 8-11, 19-22 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Kokie et al. and further in view of Nishida et al.(US#4,996,600), because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., and Kokie et al., and Nishida et al. does not teach or even fairly suggest all the limitations of independent claim 12, nor does it teach or suggest all the limitations of dependent claims 8-11, 19-22 depending, respectively, thereon. Sauer et al., and Kokie et al have been discussed above. That discussion is applicable here.

The combination of Sauer et.al., Kokie et al. and Nishida et al. does not teach or even fairly suggest all the limitations of amended independent claim 1 or of amended independent claim 12, nor does it teach or suggest all the limitations of dependent claims 8-11 and 19-22 depending, respectively, thereon. Sauer et.al., Kokie et al., and Pain et al. have been discussed above. That discussion is applicable here. Applicant respectfully asserts that since the Sauer et al. circuit does not teach or even fairly suggests the "plurality of direct injection unit cells" as recited in independent claims 1 12, 23, and 34, the man skilled in the art would not have been motivated to combine Nishida et al, Kokie et al. and Pain et al. with Sauer et

al., as there would be no motivation to combine the circuits taught by Nishida et al., Kokie et al. and Pain et al. with the circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 25, 36 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Pain et al.

Applicants respectfully traverse the rejection of claims 25, 36 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Pain et al., because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., and Pain et al., does not teach or even fairly suggest all the limitations of amended independent claim 23, and 34 nor does it teach or suggest all the limitations of dependent claims 26 and 36 depending, respectively, thereon. Sauer et al. has been discussed above. That discussion is applicable here.

Applicant respectfully asserts that since the Sauer et al. circuit does not teach or even fairly suggest the "plurality of direct injection unit cells" as recited in amended independent claims 23, and 34, the man skilled in the art would not have been motivated to combine Pain et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Pain et al. with the circuit of Sauer et al. Accordingly, Applicant respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicant respectfully asserts that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 28, 29, 39, 40 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and Pain et al., and further in view of Nishida et al.

Applicants respectfully traverse the rejection of claims 28, 29, 39, 40 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. and pain et al., and further in view of Nishida et al. because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., Pain et al., and Nishida does not teach or even fairly suggest all the limitations of amended independent claim 23, and 34 nor does it teach or suggest all the limitations of dependent claims 28-29 and 39-40 depending, respectively, thereon. Sauer et al. and Pain et al. have been discussed above. That discussion is applicable here.

Applicant respectfully asserts that since the Sauer et al. circuit does not teach or even fairly suggest the "plurality of direct injection unit cells" as recited in amended independent claims 23, and 34, the man skilled in the art would not have been motivated to combine Pain et al. and Nishida et al. with Sauer et al., as there would be no motivation to combine the circuits taught by Pain et al. and Nishida et al. with the circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In the Office Action, the Examiner rejected claims 30-33, 41-44 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Nishida et al.

Applicants respectfully traverse the rejection of claims 30-33, 41-44 under 35 U.S.C. § 103(a), as being unpatentable over Sauer et al. in view of Nishida et al. because a prima facie case of obviousness has not been established.

In order to establish a showing of prima facie obviousness, the Examiner must show that all the elements of the claimed invention are taught by the cited references and that there would have been motivation to combine them to form the claimed invention.

The combination of Sauer et.al., and Nishida does not teach or even fairly suggest all the limitations of amended independent claim 23, and 34 nor does it teach or suggest all the

limitations of dependent claims 30-33 and 41-44 depending, respectively, thereon. Sauer et al. has been discussed above. That discussion is applicable here.

Applicant respectfully asserts that since the Sauer et al. circuit does not teach or even fairly suggest the "plurality of direct injection unit cells" as recited in independent claims 23, and 34, the man skilled in the art would not have been motivated to combine Nishida et al. with Sauer et al., as there would be no motivation to combine the circuits taught Nishida et al. with the circuit of Sauer et al. Accordingly, Applicants respectfully assert that the Examiner also failed to show a motivation to combine the above references to form the invention as claimed. Accordingly, Applicants respectfully assert that this rejection is now moot and should be withdrawn.

In view of the foregoing amendments and remarks, all pending claims, claims 1-44 are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Petition For Three-Month Extension Of Time Under 37 CFR 1.136(a)

The period for responding to the instant Notice was set to expire on June 9, 2006. Applicant hereby requests that the period for responding to the instant Office Action be extended by three (3) months, so as to expire on September 9, 2006, which, being a Saturday, is extended to Monday, September 11, 2006. Accordingly, this Amendment is being timely filed.

The fee for a Petition for a Three-Month Extension of Time is One Thousand and Twenty Dollars ($1,020.00) dollars for a large entity. The United States Patent and Trademark Office is hereby authorized to charge Deposit Account 501380 in the amount of

$1,020 and any additional fee which is necessary in connection with the filing of this response and petition.

Favorable action on this response and petition is courteously solicited.

Respectfully submitted,

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Representative for Applicant(s)
Registration No. 45,148

Dated: September 11, 2006

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readout having capacitive transimpedance amplifier input circuit (discussed earlier), common TDI channel bus, and fill-and-spill[29] input to a sidecar SCCD TDI. This scheme integrates CMOS and CCD processes for much on-chip signal processing in very fine orthoscan pitch.[30]

The readout conversion factor, i.e., volts out per electrons in, for the sidecar CTIA scheme is

$$S_V = \frac{\Delta V}{e^-} = \frac{C_{FIS}}{C_T} A_{V_1} A_{V_2} \frac{q}{C_{out}} \tag{4}$$

where C_{FIS} is the fill-and-spill gate capacitance, C_T is the integration/feedback capacitance, A_{V_x} characterizes the various source follower gains, and C_{out} is the sense node capacitance at the CCD output. The ratio of C_{FIS} to C_T sets a charge gain that allows design-tailoring for dynamic range management or low input-referred noise. High charge-gain yields read noise that is limited by the input circuit and not by the transfer noise[31] of the high-carrier-capacity SCCD.

MOSFET bucket brigades are also used as TDI registers since simpler, all-MOS designs and processes can be used. Advantages include compatibility with standard MOS and CMOS, and capability for external clocking using 0–5 V, CMOS-compatible clock levels. The latter potential advantage is mitigated in the sidecar TDI scheme by appropriately sizing the SCCD registers and the charge gain to yield the desired CCD clock levels, for example. Disadvantages include higher TDI register noise due to kTC being added at each transfer and limited signal excursion.

Output Circuits. Output circuitry is usually kept to a minimum to minimize power dissipation. Circuit design thus tends to focus on the trades between voltage-mode and current-mode output amplifiers, although on-chip signal processing is increasing, including low-speed A/D conversion, switched-capacitor filtering,[32] and on-chip nonuniformity correction. Voltage-mode outputs offer better S/N performance across a wider range in backgrounds for a given readout transimpedance. Current-mode outputs offer wider bandwidth and better drive capability.

Detector Interface: Input Circuit. After the incoming photon flux is converted into a signal by the detector, it is coupled into the readout via a detector interface circuit.[33] Signal input is optical in a monolithic FPA, so signal conditioning is limited. In hybrid FPAs and some composite material monolithics, the signal is injected electrically into the readout. The simplest input schemes offering the highest mosaic densities include direct detector integration (DDI) and direct injection (DI). More complex schemes trade simplicity for input impedance reduction [buffered direct injection (BDI) and capacitive transimpedance amplification (CTIA)], background suppression (e.g., gate modulation), or ultralow read noise with high speed (CTIA). We briefly describe the more popular schemes and their performance. Listed in Table 1 are approximate performance-describing equations for comparing the circuits schematically shown in Fig. 9.

Direct Detector Integration. Direct detector integration (Figure 9*a*), also referred to as source follower per detector (SFD), is used at low backgrounds and long frame times (frame rates typically ≤15 Hz in large staring arrays). Photocurrent is stored directly on the detector capacitance, thus requiring the detector to be heavily reverse-biased for adequate dynamic range. The changing detector voltage modulates the gate of a source follower whose drive FET is in the cell and whose current source is common to all the detectors in a column or row. The limited cell constrains the source followers' drive capability and thus the bandwidth.

The DDI unit cell typically consists of the drive FET, cell enable transistor(s), and reset transistor(s). A detector site is read out by strobing the appropriate row clock, thus enabling the output source follower. The DDI circuit is capable of read noise in the range of 20 to 50 rms e-per pixel.

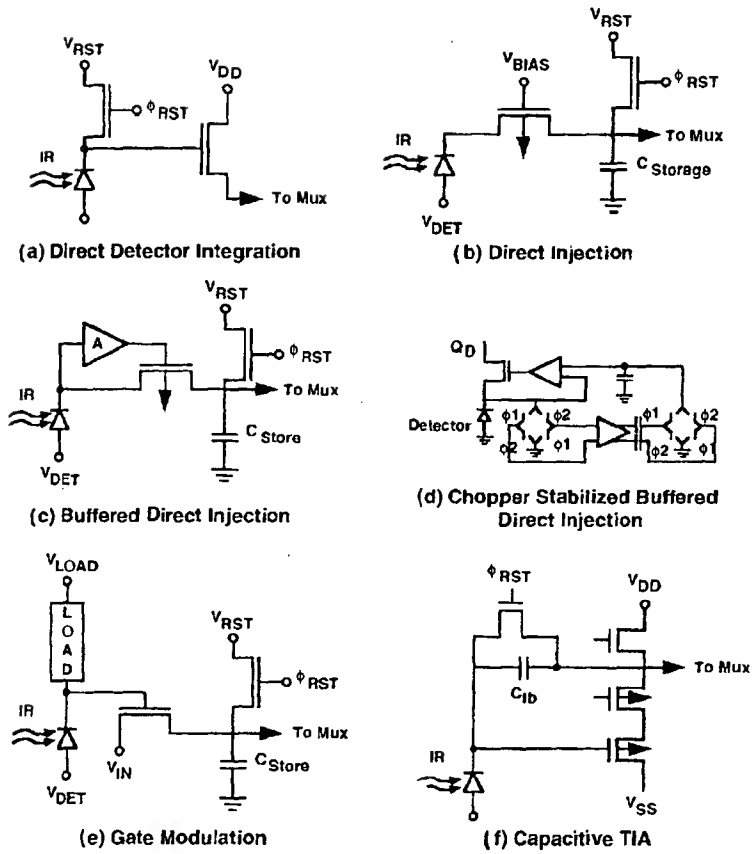


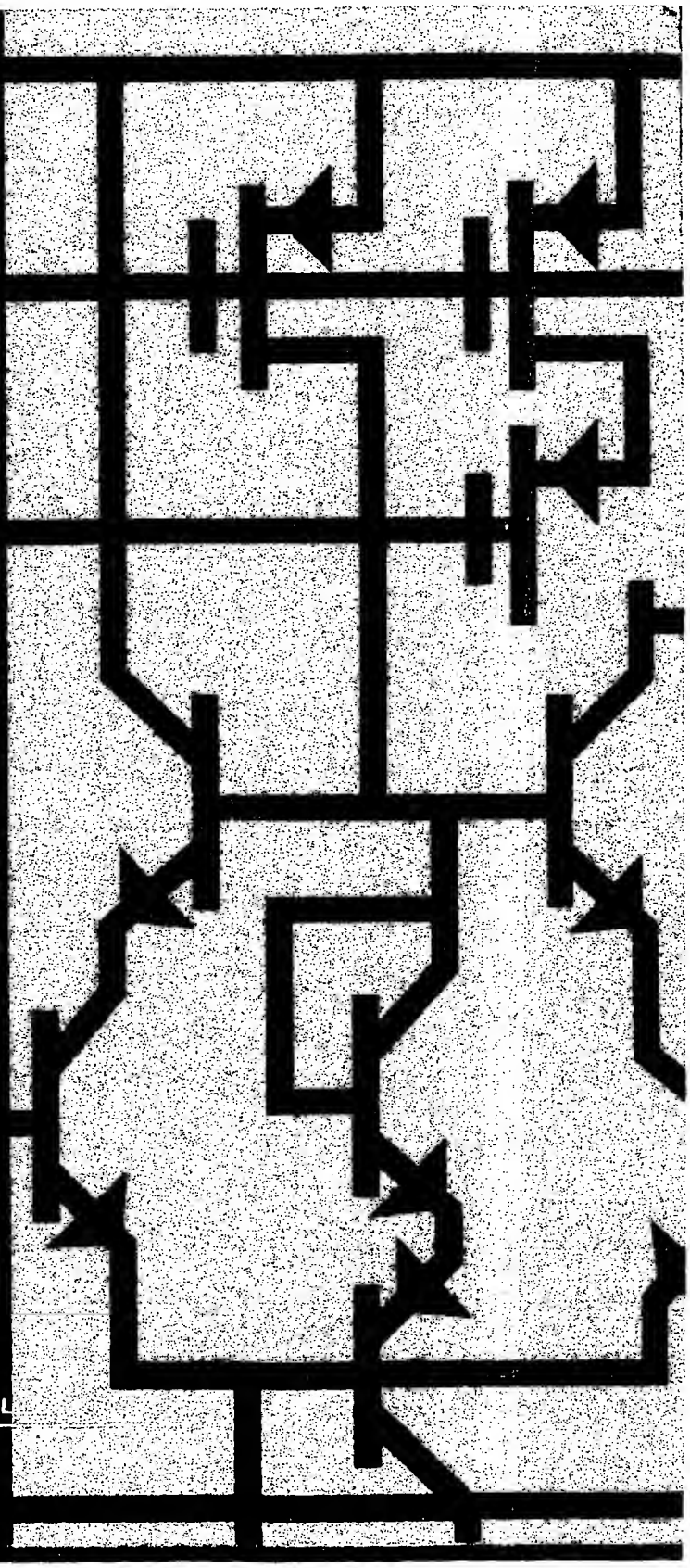
FIGURE 9 Hybrid FPA detector interface circuits.

Direct Injection. Direct injection (Fig. 9*b*) is perhaps the most widely used input circuit due to its simplicity and high performance. The detector directly modulates the source of a MOSFET. The direct coupling requires that detectors with p-on-n polarity, as is the case with InSb and most photovoltaic LWIR detectors, interface p-type FETs (and vice versa) for carrier collection in the integration capacitor. In surface channel CCDs, the FETs drain is virtual, as formed by a fully enhanced well, and doubles as the integration capacitor.

Practical considerations, including limited charge-handling capacity, constrain the DI input to operation with high-impedance MWIR or limited cutoff ($\lambda_c \leq 9.5\ \mu m$) LWIR detectors. The associated background photocurrent for the applications where direct injection can be used mandates that the DI FET operate subthreshold.[34] The subthreshold gate transconductance, g_m, is independent of FET geometry:[35]

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)\Big|_{V_{DS}=\text{constant}} = \frac{q\left(\eta_{\text{inj}}\left\{I_{\text{photo}} + \dfrac{V_{\text{det}}}{R_{\text{det}}} - I_{\text{det}_0}\left(e^{(qV_{\text{det}}/n\text{det}kT)} - 1\right)\right\}\right)}{nkT} \approx \frac{qI_D}{nkT} \tag{5}$$

DESIGN OF ANALOG INTEGRATED CIRCUITS AND SYSTEMS



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points beyond frequency f_m (see Fig. 4-18*e*). From that frequency on, the experimental data points tend to go toward the origin, rather than to r_B on the real axis. This is a result of the distributed character of r_B over both junction capacitances. Frequency f_m can thus be used as an upper limit of validity of the simple hybrid-π model presented (Getreu 1976).

Similarly, all three diagrams for the gain A_v, the input impedance Z_{in}, and the output impedance Z_{out} can be evaluated for all circuit parameters (R_S, R_L, r_π, C_π, C_μ, C_o, and g_m) as variables. This gives rise to 21 diagrams for a bipolar transistor, single-transistor amplifier stage.

In this amplifier stage, the emitter is taken as a reference (or small-signal ground). Therefore, this transistor is connected in a so-called common-emitter configuration. However, the same transistor can also be used with its collector connected to the reference (common-collector configuration), or with its base connected to the reference (common-base configuration). This gives rise to an additional 42 diagrams. Not all the diagrams are independent and not all are equally important. We will discuss only a few of them in detail, but will use others in the exercises.

In the common-collector configuration, the transistor is used as an emitter follower. This latter term is more common among designers. On the other hand, a more common name for a bipolar transistor in the common-gate configuration is a cascode transistor. We will discuss this nomenclature in Secs. 4-3 and 4-4.

As with a bipolar transistor, a MOS transistor (or JFET) can be connected with its drain to the reference (common-drain or source follower), or with its gate to the reference (common-gate or cascode configuration). They give rise to another 36 diagrams (r_π is not present). Many of the diagrams are similar to those of a bipolar transistor. We will study some in more detail because they will help us understand the role of each different configuration and each transistor parameter.

4-3 SOURCE AND EMITTER FOLLOWERS

In the previous section, a MOST has been applied in a common-source configuration, in order to generate gain and bandwidth. However, gain is not the only function to be realized. Quite often an impedance must be transformed or converted. Both types of impedance conversion occur: from high to low and vice-versa. In this section the impedance down converter stage is analyzed. Its goal is to provide buffering between input and output node. The ideal model of such a converter simply consists of an isolated input node (see Fig. 4-19*a*), followed by a voltage generator with unity gain. It is ideal because the gain is unity, the input impedance is infinity, and the output impedance zero.

In order to illustrate the converter's buffering capability, it is included in the first-order circuit of Fig. 4-19*b*. The cutoff frequency of this circuit is determined by time constant $R_{IN}C_L$. After the ideal buffer is inserted (see Fig. 4-19*c*), the time constant has become zero, which extends the frequency performance of that circuit to infinity.

We will now examine how a source (emitter) follower can be an ideal buffer. For the discussion the same models and analysis techniques are used as in the previous section. We start with the source follower.

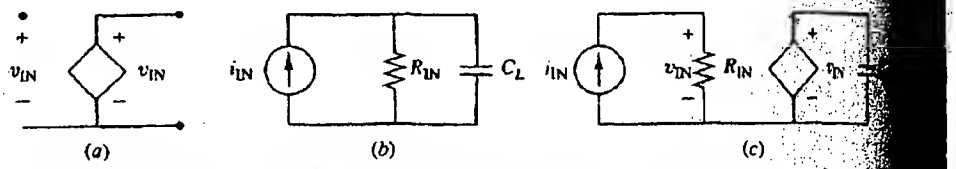


FIGURE 4-19 Model of ideal buffer (*a*) first-order circuit (*b*) without buffer; (*c*) with buffer.

4-3-1 Source Followers

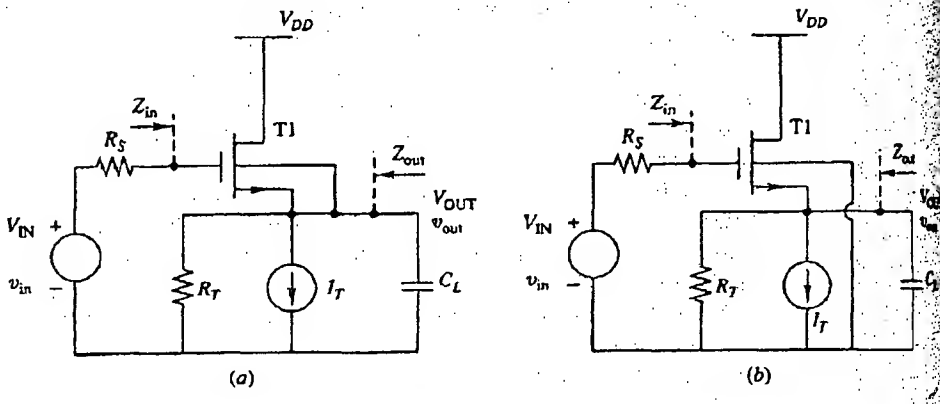
The configuration of the source follower is shown in Fig. 4-20*a* and 4-20*b*. Both are common-drain configurations because the drain is connected to the positive power supply, which is ground for small signals. The input is at the gate and the output is the source. The transistor is biased at current I_T by a current source with high, but finite, output resistance R_T. The load is represented by capacitance C_L.

The substrate can be connected to the source (Fig. 4-20*a*) or to DC ground (Fig. 4-20*b*). The first configuration is only possible for an *n*MOST in a *p*-well CMOS process and for a *p*MOST in an *n*-well CMOS process. The first configuration is easier to analyze and therefore is discussed first.

Normally, the DC input voltage V_{IN} is provided by the previous circuit. It is also possible to bias the gate by means of resistors (see Fig. 4-20*a*), although this is not common for discrete circuits. Note that the output voltage is always at a lower DC voltage than its input. This circuit can also be used for DC level shifting. Therefore we will examine this function before we explore gain, input, and output impedance.

DC Level Shift The DC level shift from input to output is easy to calculate from first-order transistor characteristics. It is the V_{GS} of transistor T1, operating at current

FIGURE 4-20 (*a*) Source follower with zero V_{BS} and (*b*) source follower.



I_T. It is given by (Fig. 4-20*a*):

$$V_{IN} - V_{OUT} = V_{T0} + \sqrt{\frac{I_T}{K'W/L}} \tag{4-52}$$

This value can be set at any specific value larger than V_{T0}, by setting the aspect ratio W/L and K', after the current I_T has been selected.

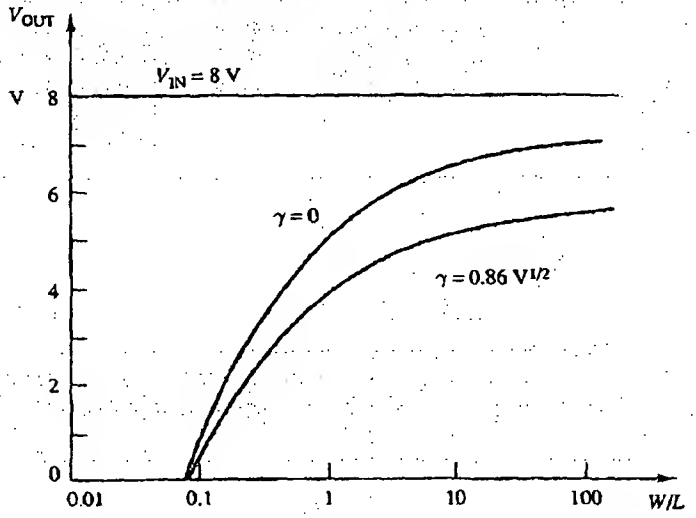
When the bulk is connected to ground (Fig. 4-20*b*), the transistor has a bulk-source polarization V_{BS}, which equals V_{OUT}. It increases the value of V_{T0} (see Chap. 1). The DC level shift is derived in Eq. (1-31*b*), then is given by

$$V_{IN} - V_{OUT} = V_{T0} + \gamma\left(\sqrt{2\phi_F + V_{OUT}} - \sqrt{2\phi_F}\right) + \sqrt{\frac{I_T}{K'W/L}} \tag{4-53a}$$

where γ is the bulk polarization factor, and $2\phi_F \approx 0.6$ V. is In this case, the DC level shift is larger, and also depends on the actual value of the output voltage. The DC output voltage is now a nonlinear function of the DC input voltage.

In both cases, the DC output voltage as plotted versus W/L in Fig. 4-21 for $I_T = 250\ \mu A$, $V_{T0} = 1$ V, $K' = 30\ \mu A/V^2$, $2\phi_F = 0.6$ V and $\gamma = 0.86\ V^{1/2}$ where $V_{IN} = 8$ V. For small values of W/L, the DC level shift becomes too large to be accommodated by the input voltage. The current source does not have sufficient output voltage to be operational. In this area the curve is denoted by a dashed line in Fig. 4-21.

FIGURE 4-21 Output voltage of source follower for $V_{in} = 8$ V and variable W/L.



As we can see, the source follower is an attractive level shifter. All DC voltages can be reached with easy control by means of W/L. It plays an important role in BICMOS for exactly this reason.

Low-Frequency Impedance Conversion For small-signal analysis, the transistor must be replaced by its small-signal equivalent, as shown in Fig. 4-22*a*, which can be further simplified to the circuit of Fig. 4-22*b*.

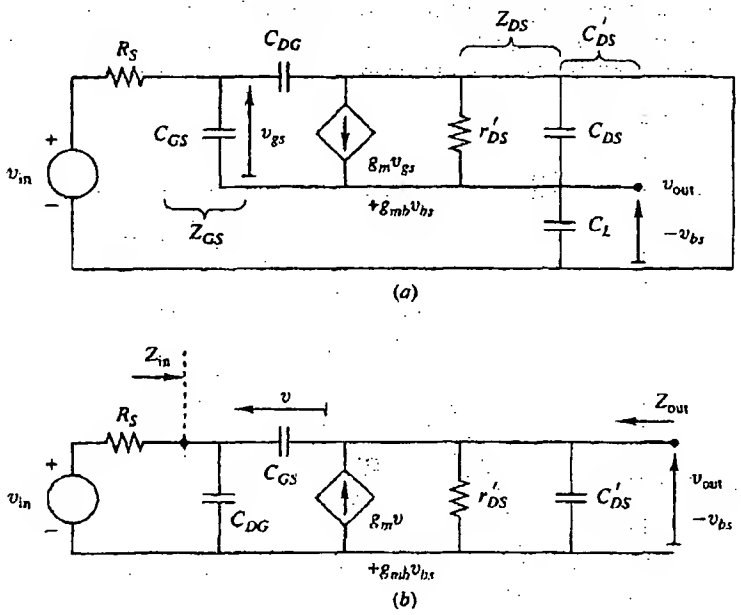
At low frequencies, all capacitances can be omitted, which leads to near ideal buffering performance: the input resistance is infinitely high. Including a large source resistance, does not make any difference.

The small-signal gain is always smaller than unity, however, but very close to unity as explained in Sec. 1-1. The output at the source "follows" the input. This is the origin of the name source follower. When the bulk is connected to ground, however, the parasitic JFET becomes active. The gain is considerably lower than unity, as given by Eq. (1-32) in Sec. 1-1.

At the output, the output resistance of the transistor r'_{DS} is put in parallel with the output resistance of the current source and the g_m and g_{mb} current generators (see Fig. 4-22*a*). As a result,

$$R_{out} = \frac{1}{g_m + g_{mb} + 1/r_{DS} + 1/R_T} \tag{4-53b}$$

FIGURE 4-22 (*a*) Small-signal equivalent circuit of source follower. (*b*) Simplified circuit.



For example, for $r_{DS} = 50$ kΩ, $R_T = 1$ MΩ, $g_m = 1$ mS, and $g_{mb} = 0.5$ mS is $R_{out} = 0.58$ kΩ. Although this is not zero, it is quite low. Thus, a resistive down conversion is realized from infinity down to 0.58 kΩ. If the bulk is connected to the source, g_{mb} drops out of Eq. (4-54), and R_{out} slightly increases to about 1 kΩ.

The importance of this impedance conversion can now be illustrated by adding a load capacitance of $C_L = 10$ pF. This value could represent a clock line over a certain distance on chip. For a source resistance of $R_S = 50$ kΩ, this capacitance would cut off all frequencies above $(2\pi C_L R_S)^{-1}$ or 0.3 MHz. With the impedance converter with $R_{out} = 0.58$ kΩ, the cutoff frequency is increased to $(2\pi C_L R_{out})^{-1}$, or 16 MHz.

High Frequency Gain Inclusion of the capacitances allows prediction of the values of gain, and input and output impedances at high frequencies. The small-signal equivalent circuit of Fig. 4-22*a* is used. This model is valid for both configurations in Figs. 4-20*a* and *b*. Only the values of C_{DS} are slightly larger when the substrate is connected to ground. Indeed, the parasitic JFET value of C_{GS} is then added to it. Load capacitance C_L can be added to C_{DS} also, since both are connected between output and small-signal ground.

The transfer characteristic of this circuit (see Fig. 4-22*b*) is of second order (three capacitances in a loop). The gain characteristic is analyzed first.

Straightforward analysis gives an expression for the gain, which is given by

$$A_v = \left\{ \frac{1 + \left(\frac{C_{GS}}{g_m}\right) s}{1 + \left[\left(1 + \frac{R_S}{r_{DS}}\right)\frac{C_{GS}}{g_m} + \frac{C'_{DS}}{g_m} + R_S C_{DG}\right] s + \left(\frac{R_S}{g_m}\right) C'^2 s^2} \right\} \tag{4-54}$$

in which C'^2 is given by Eq. (4-19*b*), using C'_{DS} instead of C_{DS}. To simplify the analysis the gain is assumed to be unity at low frequencies.

The pole-zero position plot of this expression versus g_m is given in Fig. 4-23*a*. The actual Bode diagram of $|A_v|$ is shown in Fig. 4-23*b*.

The expression of the dominant pole is given by

$$f_d = f_{c6}\left(\frac{1}{1 + \frac{g_m}{g_{mr}}}\right) \tag{4-55a}$$

with

$$g_{mr} = \left(\frac{1}{R_S}\right)\left(\frac{C_{GS} + C'_{DS}}{C_{DG}}\right) \tag{4-55b}$$

in which f_{c6} is already given in Table 4-1. For $g_m = 1$ mS, the value of $g_{mr} = 3.3$ mS.

The expression of the nondominant pole is given by

$$f_{nd} = f_{c18}\left(1 + \frac{g_m}{g_{mr}}\right) \tag{4-56a}$$

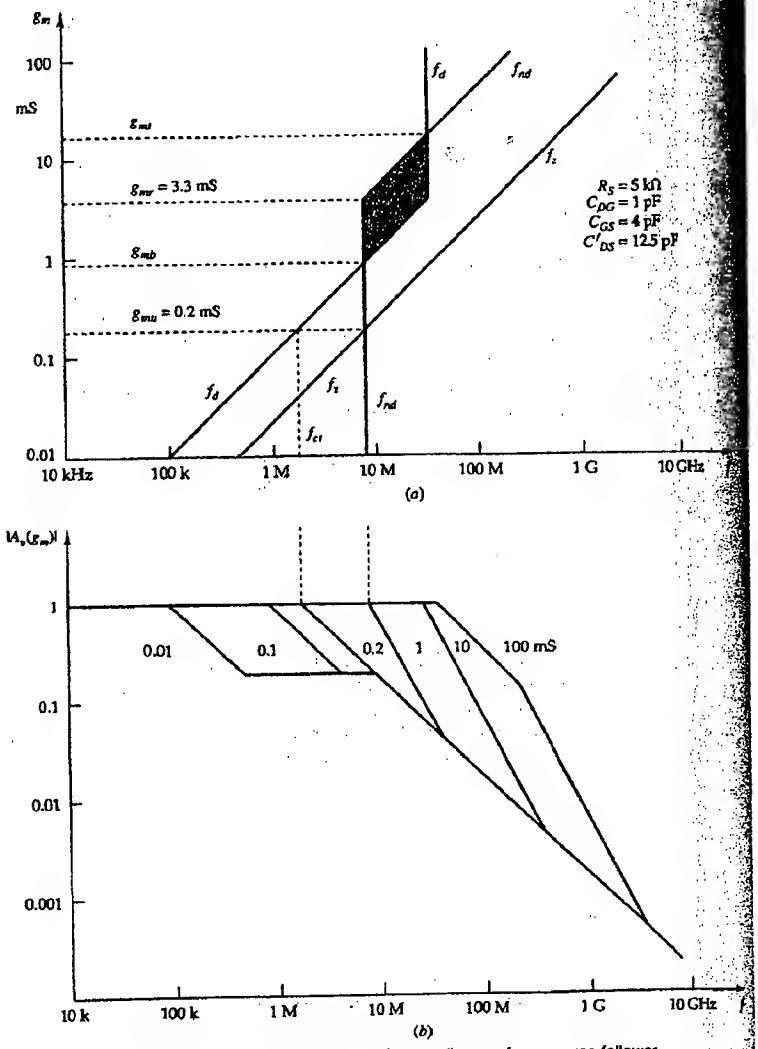


FIGURE 4-23 (a) Pole zero position plot of $A_v(g_m)$: and (b) Bode diagram for a source follower.

ground, forming a lowpass filter at the input with time constant $R_S C_{DG}$. This lowpass filter is required to avoid peaking.

Note that there is one zero proportional to g_m. It is not positive, however, it is negative. A single-pole characteristic can be obtained at the value of g_m, where this zero cancels the nondominant pole. The approximate value of g_m is given by

$$g_{mu} = \frac{1}{R_S} \tag{4-58a}$$

(see Fig. 4-23*a*).

Its value is 0.2 mS. At this value of g_m and for $C_{DG} = C_{DGt}$, the cutoff frequency is given by

$$f_{ct} = \frac{1}{2\pi R_S (2C'_{DS})} \tag{4-58b}$$

Its value equals 9.6 MHz (for $C_{DG} = 1$ pF) and 8.1 MHz (for $C_{DG} = 3$ pF).

This value of g_{mu} can be realized easily at low currents. For large values of R_S, however, this rule is impractical. The transconductance cannot be lowered to that level.

with $$f_{c18} = \frac{C_{GS} + C'_{DS}}{2\pi R_S C'^2} \tag{4-56b}$$

For values of g_m smaller than g_{mr}, f_{nd} equals f_{c18}, which is 7.9 MHz ($C'^2 = 66.5$ pF^2).

It is interesting to note, however, that the lines of the poles cross each other. The enclosed area is denoted by hatch marks in Fig. 4-23*a*. Since the nondominant pole cannot occur at frequency values lower than the dominant pole, something is wrong with the approximations. The reason is that for values of g_m, (which correspond with the hatched area), two complex poles occur at the frequencies represented by the thick line connecting the extremes of the hatched area.

Complex poles lead to peaking, and thus must be avoided. Peaking is maximum in the middle at $g_m = g_{mr}$ (3.3 mS), but starts at the bottom of the hatched area at g_{mb} and continues up to its top at g_{mt}, (calculated as in the example of App. 4-1). The ratio of g_{mt} (13.3 mS) to g_{mb} (0.8 mS) is easily calculated to be

$$\frac{g_{mt}}{g_{mb}} = 1 + \frac{C_{DGt}}{C_{DG}} \tag{4-57a}$$

with $$C_{DGt} = \frac{C_{GS}C'_{DS}}{C_{GS} + C'_{DS}} \tag{4-57b}$$

Ratio g_{mt}/g_{mb} equals 16 in the example. Obviously, this ratio depends on the load capacitance C'_{DS} and C_{GS}, as well as on compensating capacitance C_{DG}. This ratio can never be made smaller than or equal to unity.

The hatched area is minimum as soon as C_{DG} is larger than C_{DGt}, or 3 pF in this example. Note, however, that C_{DG} is actually all the capacitance from the gate to ground, forming a lowpass filter at the input with time constant $R_S C_{DG}$. This lowpass filter is required to avoid peaking.

Note that there is one zero proportional to g_m. It is not positive, however, it is negative. A single-pole characteristic can be obtained at the value of g_m, where this zero cancels the nondominant pole. The approximate value of g_m is given by

$$g_{mu} = \frac{1}{R_S} \tag{4-58a}$$

(see Fig. 4-23*a*).

Its value is 0.2 mS. At this value of g_m and for $C_{DG} = C_{DGt}$, the cutoff frequency is given by

$$f_{ct} = \frac{1}{2\pi R_S (2C'_{DS})} \tag{4-58b}$$

Its value equals 9.6 MHz (for $C_{DG} = 1$ pF) and 8.1 MHz (for $C_{DG} = 3$ pF).

This value of g_{mu} can be realized easily at low currents. For large values of R_S, however, this rule is impractical. The transconductance cannot be lowered to that level,

about 32 MHz.

Decreasing W/L will decrease the current, but will increase the compensation capacitance and will decrease the bandwidth.

because the current becomes very small, as well. Take, for example, $R_S = 50$ MΩ. Then, $g_m < 20$ nS, which is obtained for currents around 1 nA. With a low value of drain current, current is insufficient to charge and discharge capacitance C'_{DS} (including C_L), resulting in slew rate distortion. Thus larger currents are taken. In order to avoid peaking under these conditions, capacitance C_{DG} must be increased. It then functions as a compensation capacitance, or as an input filter, as already explained.

The time constant in Eq. (4-58*b*) is obviously $R_S C'_{DS}$. It is the dominant time constant because C'_{DS} includes the large load capacitance. This dominant pole value is the same as if the output capacitance C'_{DS} were connected directly to the source resistance R_S, without an intervening transistor. In other words, the transistor, which should buffer output from input, merely causes peaking if we try to increase the bandwidth. The main culprit is, of course, the presence of C_{GS}, which directly connects output to input. We use capacitance C_{DG}, however, to stabilize (or compensate) this stage, even for values of g_m larger than g_{mu}.

For very large values of g_m, two single poles occur (see Fig. 4-23*a*), the second of which always is closely followed by the zero. All values of g_m can now be used for peaking without danger.

It can be concluded that the addition of input capacitance to C_{DG} stabilizes the source follower. It decreases the value of the dominant pole such that only one critical value of g_m is left. The minimum value of C_{DG} is given by Eq. (4-57*b*). The critical value of g_m, which is better avoided, is given by Eq. (4-55*b*).

Example 4-8

Let us design a source follower for a load capacitance of $C_L = 100$ pF. What is its minimum W/L, and/or drain current I_{DS}? What bandwidth is then achieved?

We use as parameters the values of Table 4-1. However, in order to take into account the dependence of C_{GS} and C_{DG} with W/L, we take $C_{GS} = 0.01 \times W/L$ pF and $C_{DG} = C_{GS}/4$.

Solution. We will need a large current to drive 100 pF. Thus, the transistor will have a large value of W/L. The critical value of g_m is taken from Eq. (4-55*b*) and can be expressed as $g_{mr} \approx [2/(W/L)]S$ if $C_{GS} < 100$ pF. On the other hand, the minimum value of C_{DG} is given by Eq. (4-57*b*) and can be expressed as $C_{DGi} \approx C_{GS} = 0.01\ W/L$ pF again, if $C_{GS} < 100$ pF. An optimization could be carried out, but a good compromise for a designer is $W/L \approx 200$. This yields $g_{mr} \approx 10$ mS. Let us take twice g_{mr} or $g_m = 20$ mS. The compensation capacitance is $C_{DGi} = 2$ pF. Thus it will cost us a large area to allow this large current, either in transistor size or in capacitor size! The bandwidth is determined by f_{c6}, which is a result of the 100 pF load, seeing $1/g_m$ (or 50 Ω) at the output node. Thus it is about 32 MHz.

Decreasing W/L will decrease the current, but will increase the compensation capacitance and will decrease the bandwidth.

Input Impedance The expression of input impedance of the source follower (Fig. 4-22*a*) is given by (if $g_m r'_{DS} \gg 1$):

$$Z_{in} = \left(\frac{1}{\left(C_{DG} + \frac{C_{GS}}{g_m r'_{DS}} \right) s} \right) \left(\frac{1 + j\left(\frac{f}{f_{c6}} \right)}{1 + \frac{r'_{DS} C^2 s}{C_{GS} + g_m r'_{DS} C_{DG}}} \right) \tag{4-59}$$

in which f_{c6} is given in Table 4-1.

Obviously, the input impedance is capacitive. At low frequencies, the input capacitance is about C_{DG}. Capacitance C_{GS} is bootstrapped out because of the large value of $g_m r'_{DS}$ (50 in the example). If a really high input impedance or low input capacitance is required, then C_{DG} must be reduced to below $C_{GS}/g_m r'_{DS}$ (a mere 0.06 pF).

At higher frequencies one pole and one zero are included; these nearly cancel each other.

Output Impedance The expression of the output impedance is derived from Fig. 4-20*b* with $C_L = 0$, and is given by

$$Z_{out} = \frac{1}{g_m} \left\{ \frac{1 + j\left(\frac{f}{f_{c13}} \right)}{1 + \left[\left(1 + \frac{R_S}{r_{DS}} \right) \left(\frac{C_{GS}}{g_m} \right) + \frac{C'_{DS}}{g_m} + R_S C_{DG} \right] s + \left(\frac{R_S}{g_m} \right) C'^2 s^2} \right\} \tag{4-60}$$

If $g_m r'_{DS} \gg 1$. Frequency f_{c13} is given in Table 4-1. The low-frequency value (see Eq. (4-53)) has been reduced to g_m for simplicity.

Note that the poles are the same as the gain, given by Eq. (4-54). The pole-zero position plot versus g_m, and the Bode diagram of $|Z_{out}|$ are studied in the exercises. The only important result is that values of g_m around g_{mr} (given by Eq. (4-55*b*)) should once again be avoided.

There are several other characteristics that should be studied. For example, capacitance C_{DG} is the input node capacitance of the source follower. In order to investigate how well the source follower can screen the effect of this input node capacitance, the output impedance could be examined with C_{DG} as a variable. Also, in order to investigate to what extent the source follower is able to convert high input resistances into the low output resistance of $1/g_m$, $|Z_{out}|$ could be plotted for different values of R_S. These plots are considered in the exercises.

The conclusion always holds that the main advantage of the MOST source follower is the reduction of the impedance from ∞ to $1/g_m$ up to f_{c6}, a high frequency indeed. To avoid peaking, a relation exists between R_S, g_m, and the capacitances. As a result, a minimum value is required for g_m, which is g_{mr}. A minimum value, especially, is required for input capacitance C_{DG}.

After source followers, the emitter followers are discussed in order to see how closely they can realize ideal buffering, compared to their MOST equivalents.

The excess noise factor, which gives the ratio of the equivalent input noise $\overline{dv_i^2}$ to that of the first input transistor $\overline{dv_{ie}^2}$, is then given by

$$y = \frac{\overline{dv_i^2}}{\overline{dv_{ie}^2}} \approx 1 + \frac{\overline{dv_A^2}}{\overline{dv_{ie}^2}} \tag{4-69}$$

It can be concluded that the equivalent input noise of the emitter follower of the fact that the emitter follower only provides a gain of unity and hence does not reject the noise of the next stage. For low noise applications, both the emitter follower itself and the next amplifier must be designed for low noise.

Followers are impedance-down converters. Let us now discuss impedance-up converters, or cascodes.

4-4 CASCODE TRANSISTORS

In this section the impedance-up converter stage is analyzed. This stage provides buffering between an input and an output node. The ideal model of such a converter consists of a short-circuited input node (see Fig. 4-29) followed by a current generator with unity gain. It is ideal because the gain is unity, the input impedance is zero, and the output impedance infinity.

We will now examine how a cascode configuration can be an ideal buffer. For this analysis, we will use the same models and analysis techniques as before. We start with the MOST cascode.

4-4-1 MOST Cascode

Cascode configurations are shown in Fig. 4-30. Both are common-gate configurations because the gate is connected to a positive reference voltage V_{GG}, which is ground for small signals. Normally it is derived from the positive power supply voltage by means of resistors, which are represented by an equivalent series resistor R_G.

The input is at the source and the output at the drain. The transistor is biased at current I_{IN} by a current source with high, but finite, output resistance R_T. The load is represented by capacitance C_L.

The substrate can be connected to the source (Fig. 4-30*a*) or to DC ground (Fig. 4-30*b*), in exactly the same way as in a source follower configuration.

DC Conditions First let us look at the DC conditions of the MOST cascode. The current through the transistor is determined by current source I_{IN}, which also flows

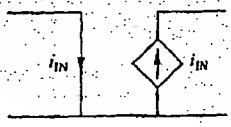


FIGURE 4-29 Model of ideal buffer

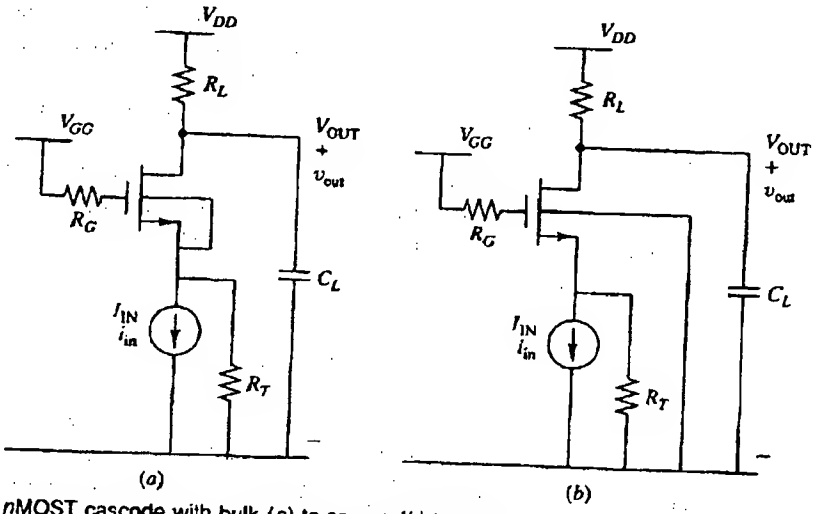
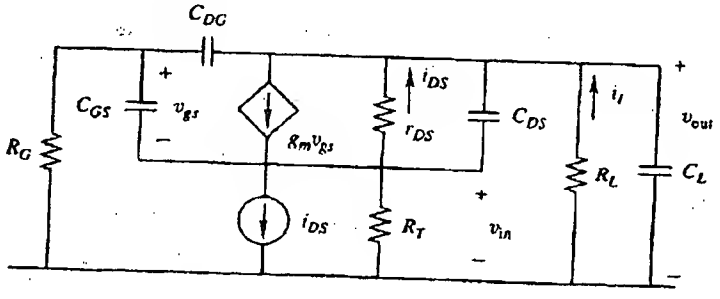


FIGURE 4-30 *n*MOST cascode with bulk (*a*) to source (*b*) to ground.

through the output resistor R_L. As a result, the output voltage is determined by the voltage drop across R_L, as given by Eq. (4-3). The DC voltage at the source follows the biasing voltage V_{GG} as for a source follower. Thus, the DC voltage drop between gate and source is also given by Eq. (4-52). In this way, the DC currents and voltages are all known.

Low Frequency Analysis To study the low-frequency performance of the cascode, let us consider its small-signal equivalent circuit illustrated in Fig. 4-31. At low frequencies all capacitances can be omitted. We now must verify whether the current gain is unity, the input resistance is small, and the output resistance large. Let us start with the current gain.

FIGURE 4-31 Small-signal equivalent circuit of cascode.



On first sight the *current gain* is unity, because all current pulled from the source must come out of the load resistor. However, close inspection of the small-signal circuit in Fig. 4-31 shows that two resistances are present that shunt the current generators $g_m v_{gs}$ and i_{in}. They are r_{DS} and R_T. A detailed analysis is required (Abidi 1990).

Application of Kirchhoff's laws allows us to write the output current i_{out} as a function of the input current i_{in}. This ratio is the current gain A_i. The output voltage v_{out}, as a function of the input current i_{in}, is then the transresistance $A_r = A_i \cdot R_L$. The current gain A_i is given by

$$A_i = \frac{i_l}{i_{in}} = \frac{R_T(g_m r_{DS} + 1)}{R_L + R_T(g_m r_{DS} + 1) + r_{DS}} \tag{4-70}$$

in which $R_T(g_m r_{DS} + 1) + r_{DS}$ in the denominator is a very large resistance (denoted by R_{Lc}). This expression is plotted in Fig. 4-32*a* and shows that for all values of R_L smaller than R_{Lc}, the current gain A_i is unity. The transresistance A_r is plotted in Fig. 4-32*b*. It increases proportionally to R_L until R_{Lc} is reached, at which point A_r reaches a constant maximum value of R_{Lc}.

Thus, for large gain, a cascode must have a large R_L. Once values are used higher than R_{Lc}, no extra gain is achieved.

In order to gain some more insight into the operation of the cascode, let us also calculate the current i_{ds} flowing through the transistor output resistance r_{DS}. This is obtained from straightforward analysis and given by

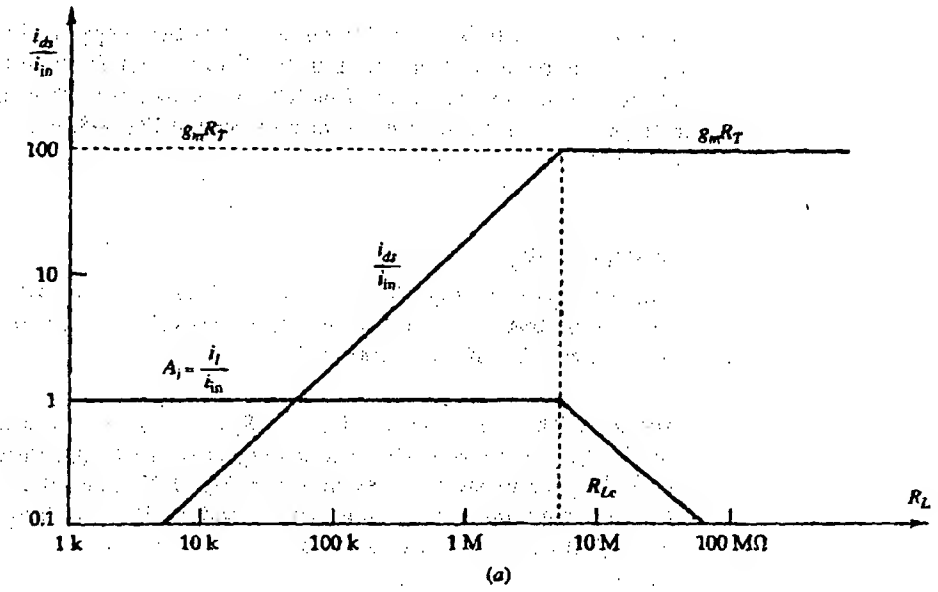
$$\frac{i_{ds}}{i_{in}} = \frac{R_T(g_m R_L - 1)}{R_L + R_T(g_m r_{DS} + 1) + r_{DS}} \tag{4-71}$$

also plotted in Fig. 4-32*a*. This clearly shows that for large values of R_L, a large current flows through r_{DS}, which is provided by the $g_m v_{gs}$ generator. It is much larger than i_{in} itself. This current will have an enormous effect on the input resistance R_{in}, calculated next.

The input resistance R_{in} is given by

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_T(R_L + r_{DS})}{R_L + R_T(g_m r_{DS} + 1) + r_{DS}} \tag{4-72a}$$

which is also plotted in Fig. 4-32*b*. It shows that for small load resistors, the input resistance is $1/g_m$, as expected. However, for large load resistors, the input resistance increases and reaches a value as high as R_T, when $R_L = R_{Lc}$. At this point, the transistor itself exhibits an input resistance infinity such that the resistance at the source is determined by the input current source's output resistance. This means that no buffering effect is obtained; the large load resistance is clearly visible at the source, through r_{DS}. Moreover, the input resistance is low (i.e., $1/g_m$) only when R_L is low. This is the casc only in some types of wide-band amplifiers. In operational amplifier type circuits, active loads are used, and hence R_L can be very large.



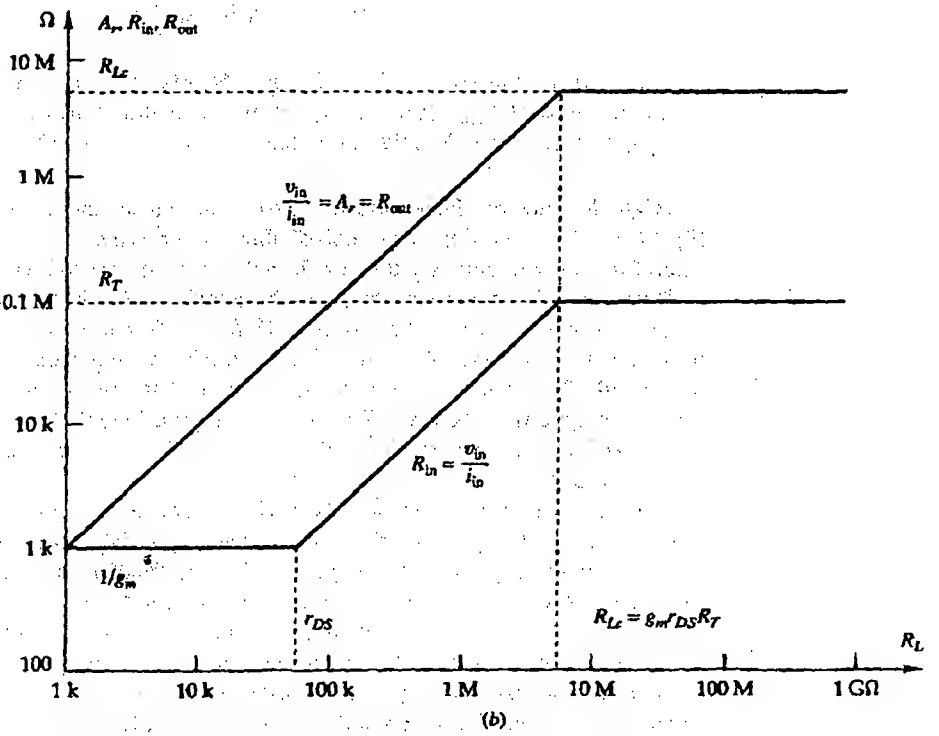


FIGURE 4-32 (*a*) Current ratios in a cascode; (*b*) resistance levels in a cascode.

The only characteristic left for discussion is the output resistance R_{out}. This resistance is the parallel combination of the load resistor R_L with the resistance at the drain looking into the transistor. This latter resistance is readily calculated to be R_{Lc}. The output resistance is thus A_r, as already seen in Fig. 4-32*b*. An example will make this clear.

Example 4-10

Plot the curves of Fig. 4-32 for the *n*MOST of Table 4-1 with the additional information that $r_{DS} = 60$ kΩ and $R_T = 100$ kΩ. What are the values of the gain A_r, R_{in}, and R_{out} if $R_L = 100$ kΩ?

Solution. The critical value of R_L is R_{Lc}. Its value is obtained from Eq. (4-70) and is $R_{Lc} = 6.16$ MΩ. This is much higher than 100 kΩ. Hence, $A_r = 100$ kΩ as well. The curves are the ones shown in Fig. 4-32. For values of R_L smaller than R_{Lc}, an approximate expression can be used for R_{in}. It is derived from Eq. (4-72*a*) by neglecting R_L in the denominator and is given by

$$R_{in} \approx \frac{1}{g_m}\left(1 + \frac{R_L}{r_{DS}}\right) \tag{4-72b}$$

Since the second term is 2.66, R_{in} is 2.66 kΩ. Note that this expression shows the presence of $1/g_m$ more explicitly. It is a useful expression to remember when designing cascodes. Finally, the value of R_{out} is simply 100 kΩ as well.

High Frequency Performance Now all capacitances must be included in Fig. 4-31. This gives us a system of third order. Thus it is not easy to evaluate. Therefore, we will simplify the circuit before we attempt to analyze it.

Resistance R_G can be made small by addition of a large (external) capacitance to ground at the gate of the cascode. If $R_G = 0$, capacitance C_{DG} can be added to C_L, which becomes C'_L, and C_{GS} becomes the input capacitance from source to ground. This is now a second-order system that can be analyzed with pole-zero position diagrams, as before. However, we will calculate the poles assuming that only one capacitance is present. We will later decide if we want to draw a full pole-zero position plot.

For capacitance C'_L, the pole is easy to calculate because the time constant is simply $R_{out}C'_L$. The pole position plot with R'_L as variable is derived from Fig. 4-32*b* and is shown in Fig. 4-33. The larger the R'_L, the smaller the pole frequency. Finally, note that the curves of Fig. 4-33 have been calculated for the numerical values of Example 4-10, with $C'_L = 10$ pF, $C_{GS} = 4$ pF, and $C_{DS} = 2.5$ pF.

Another pole easy to calculate is that associated with C_{GS}. This capacitance is connected from source to ground. Thus it generates a pole with R_{in}. Its position is again derived from Fig. 4-32*b* and is also shown in Fig. 4-33. It occurs at much higher frequencies than that of C'_L, except for very low values of C'_L. Both poles coincide

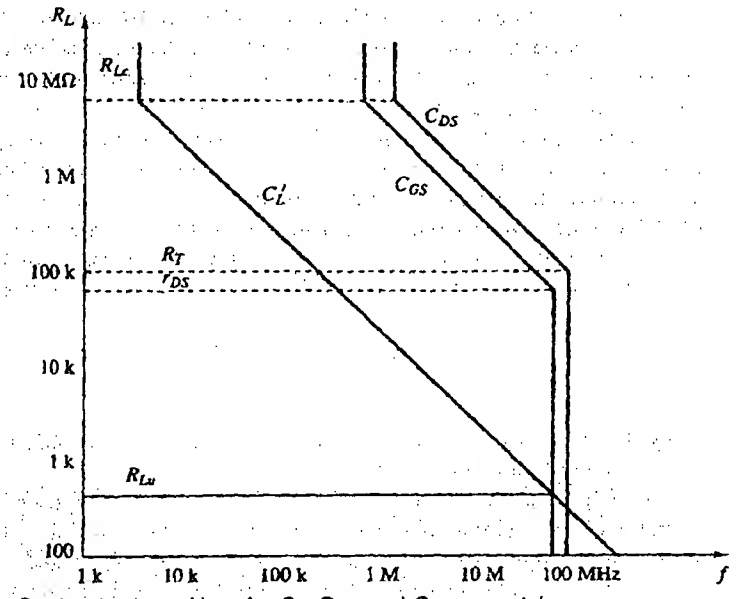


FIGURE 4-33 Dominant pole positions for C_L, C_{GS}, and C_{DS} separately.

at the value of R'_L, which is denoted by R_{Lu} and given by

$$R_{Lu} = \frac{1}{g_m}\left(\frac{C_{GS}}{C'_L}\right) \tag{4-72c}$$

At this value a complex pole pair occurs. It is a result of resonance between C_{GS} and C'_L. Therefore, this range is to be avoided.

The pole due to C_{DS} is more difficult to calculate. The easiest way to calculate the resistance is seen by C_{DS} in Fig. 4-31 at low frequencies. This is r_{DS} in parallel with a resistance, which is easily calculated to be $1/g_m\ (1 + R_L/R_T)$. The resulting pole positions are given in Fig. 4-33. The pole due to C_{DS} is of the same order of magnitude as that of C_{GS}. Together they form the nondominant pole for most values of R_L, except around R_{Lu}, where both C_{DS} and C_{GS} contribute to the complex pole pair.

It is clear from the pole-zero position plot of Fig. 4-33 that a dominant pole can be recognized for most values of R_L. This is not the case around R_{Lu}, where two complex poles occur. Therefore the full analysis with pole-zero position diagrams is not carried out.

4.12 Bipolar Transistor Cascodes

Substitution of the *n*MOST by an *npn* bipolar transistor in the cascode configuration of Fig. 4-30*a* gives us a bipolar transistor cascode. Rather than going through a full analysis again, we will limit the discussion to the differences between both.